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~~TRANSMISSION METHOD AND TRANSMISSION SYSTEM~~

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The present invention is directed to a method for the transmission of data in an ATM transmission system as well as to an ATM transmission system, particularly an ATM broadband transmission system.

Description of the Related Art

Many new transmission or~~, respectively,~~ switching principles for various types of transmission in communication networks have been developed during the course of the rapid development of communications technology in recent years. The ~~What is referred to as the~~ STM transmission principle (synchronous transfer mode) deals with ~~is a matter of~~ a synchronous transfer or~~, respectively,~~ transmission method in which the ~~. The~~ data of various data channels are ~~thereby~~ serially transmitted within different time slots, and ~~whereby~~ the individual time slots are combined into frames. A frame synchronization word is transmitted for the synchronization of each and every frame, so that each time slot of a frame allocated to a specific data channel exhibits a fixed time spacing from the frame synchronization word. Each time slot can contain a relatively small number of bits, for example 8 bits, and appears at constant time intervals. However, highly different bit rates cannot be uniformly governed with the assistance of this STM principle, i.e., different communication networks for different bit rate ranges would have to be provided given application of the STM principle, particularly given the currently desired broadband signal transmission. A uniform digital broadband communication network (broadband integrated services digital network, BISDN) cannot be realized with the assistance of the STM principle.

The ~~What is referred to as the~~ ATM transmission or~~, respectively,~~ switching principle (asynchronous transfer mode) is significantly more flexible compared a2 ~~thereto~~. According to this ATM principle, cells that contain 53 octets / ~~or, respectively,~~ bytes as payload information as a standard are ~~now~~ transmitted instead of the time slots of the STM principle. These ATM cells are transmitted with a constant transmission rate dependent on the band width of the transmission medium. Dummy cells are used when no messages are to be transmitted. A ~~What is referred to as a~~ "header", which contains

the control or~~, respectively,~~ address information for the corresponding cell, is attached to the information field of every cell, which contains the actual payload information.

Figure 3a shows an illustration for explaining the ATM principle. As shown in Figure 3a, a plurality of cells Z are successively transmitted (in ~~arrow direction~~) from a sender to a receiver. As has already been set forth, each cell thereby comprises a header with address or control information as well as an information field with the actual payload information. According to the defined standard, the information field comprises 48 octets, and ~~whereas~~ the header comprises 5 octets, so that each cell is formed by 53 octets ~~or, respectively,~~ bytes. Additional (header) octets can be attached to this cell format which are ~~, these being~~ capable of being employed for the routing of the cell upon transmission of the cell from a sending subscriber to a receiving subscriber.

In newer ATM broadband transmission systems or~~, respectively,~~ communication networks, the data streams between the individual transmission and reception assemblies are optically transmitted via light waveguides. These ATM broadband communication networks ~~thereby~~ allow an extremely high data throughput that~~, however,~~ cannot -- due to technological limitations -- be processed by the switching elements that are thereby employed and that are usually fashioned in CMOS technology. ~~The~~ data to be transmitted are therefore supplied in parallel to transmission modules via a plurality of data lines and transmitted by the transmission modules serially multiplex via the light waveguides to reception modules, which in turn divide the serial ATM data stream onto corresponding, parallel data channels at the output side for further processing.

This principle is shown in Figure 3b. An ~~What is referred to as an~~ optical ATM link serving as transmitter receives digital data of a plurality of data channels K_0-K_n. Further, the sender S is supplied with a clock signal T. Dependent on the clock signal T, the sender S thus respectively reads n + 1 bits in in parallel, and converts these bits into a serial, multiplexed ATM data stream D having a correspondingly higher data transmission rate, and ~~whereby~~ this data stream D is optically transmitted to a receiver E. This receiver E parallelizes the received, serial data streams D, and in turn

outputs it in parallel via data channel lines K_0-K_n of the output side together with a clock signal T.

It is apparent on the basis of the above description that the demultiplexing of the serial data stream D in the receiver E represents a specific problem. For demultiplexing the data stream D, the receiver E must known which bit of the serial data stream D is to be allocated to which data channel K_0-K_n of the output side. For this purpose, known solutions provide that additional synchronization information be attached to the actual serial data stream D at the transmission side, these additional synchronization information being interpreted in the receiver E and defining the allocation of the digital information transmitted in the serial data stream D to the individual data channels K_0-K_n of the output side. Thus, for example, additional synchronization information can be attached with the assistance of an encoding implemented in the sender S, particularly a block encoding. As a result of the block encoding in the sender S, a redundancy is attached to the actual serial data stream D, as a result of which ~~whereof~~ the serial data rate of the data stream D rises. On the other hand, a relatively high circuit outlay is required in the receiver E in order to be able to interpret the synchronization information attached to the serial data stream D. This ~~all~~ results in ~~therein that~~, for example, no inexpensive standard lasers can be utilized for the transmission of the data of the input-side data channels K_0-K_n.

An example for the demultiplexing of a serial data stream is disclosed in ~~can be taken from~~ United States Letters Patent 5,579,324, in which ~~The~~ arriving bit stream is ~~thereby~~ synchronized by a control block, resulting in a significant ~~as a result whereof a not inconsiderable~~ outlay in the demultiplexing ~~arises~~ at the reception side.

Further, more Swiss Letters Patent 682 277 discloses methods for the synchronization of a serial ATM bit stream, which particularly addresses ~~How~~ the cell boundaries of a serial ATM bit stream can be identified ~~is thereby particularly addressed~~. However, how a demultiplexing of a serially transmitted data stream is to be efficiently undertaken at the reception side is not addressed in this reference ~~here~~.

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SUMMARY OF THE INVENTION 3a

The present invention is therefore based on the object of creating a transmission method for an ATM transmission system as well as a corresponding ATM transmission system, ~~whereby~~ in which a receiver-side demultiplexing of the serially transmitted data stream is possible with relatively simple circuit-oriented outlay. In particular, a correct demultiplexing of the serial data stream should be possible without attaching additional synchronization information and, thus, without attaching redundancy.

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INS a6 9b ~~According to the present invention, this object is achieved by a method having the features of claim 1 as well as by an ATM transmission system having the features of claim 14. The subclaims respectively describe advantageous and preferred exemplary embodiments of the present invention that in turn contribute to an optimally simple data transmission.~~

According to the present invention and in agreement with the ~~Prior~~ Related Art, the digital data of the parallel data channels present at the transmission side continue to be converted bit-by-bit into a serial ATM data stream, i.e., continue to be multiplexed, where~~by~~ the serial data of the ATM data stream are transmitted in the form of the initially described ATM cells. According to the present invention, however, a characteristic bit sequence with whose assistance the beginning of the corresponding ATM cell in the serial data stream can be acquired at the receiver side is transmitted within each cell. This characteristic bit sequence is preferably a matter of a synchronous octet that is already transmitted with every ATM cell, so that the beginning of the corresponding ATM cell can be recognized by monitoring the received data stream for the appearance of this synchronous octet, and, thus, the information of the serial data stream can be correctly parallelized and divided onto corresponding data channels of the output side.

To this end, the digital data of the data channels supplied parallel at the input side are combined bit-by-bit into data units that form the ATM cells to be respectively transmitted. Each ATM cell transmitted with the assistance of the serial data stream thus contains a plurality of data units that respectively comprise an identical plurality of bits of each and every parallel data channel. It is fundamentally conceivable that two or more bits are transmitted with each data unit from each data channel. In practice, however, the parallel data channels adjacent at the input side are sampled bit-by-bit, so that each data unit of each data channel comprises only one bit. The corresponding bit of a data channel is always situated at the same location within each data unit, so that the individual bits can be easily divided onto the parallel, output-side data channels at the reception side after identification of the beginning of a data unit. The employment of respectively four data channels of the input side and output side is especially advantageous since the data of the data channels can be combined into half-bytes in four-bit fashion, ~~whereby~~ by which each half-byte forms an above-described data unit of the ATM cell to be transmitted. Each octet of an ATM cell, accordingly, comprises two of these half-bytes. The data of each ATM cell are thus serially transmitted from the transmitter to the receiver in half-byte fashion.

The inventively proposed evaluation of the characteristic bit sequence of the cell, which is already transmitted with the cell and is usually formed by the first byte of each ATM cell, thus makes it possible that no additional signals or synchronization information for the channel allocation are required for the demultiplexing of the receiver side. An increase in the data rate of the optically transmitted, serial data stream together with the above-described associated disadvantages connected ~~therewith~~ can thus be avoided. The invention thus enables a data transmission according to the ATM transmission principle with relatively little circuit outlay and allows the employment of smaller module sizes for the transmitter or ~~respectively,~~ receiver modules. Further, more the transmission is possible with a lower dissipated power, and the costs can be reduced as a result of the lower circuit outlay.

The invention is particularly directed to the transmission of data within an ATM switching system.

BRIEF DESCRIPTION OF THE DRAWINGS

The invention is explained in greater detail below with reference to the attached drawing on the basis of a preferred exemplary embodiment. ~~Thereby shown, are:~~

Figure 1 is a schematic illustration of a preferred exemplary embodiment of the inventive ATM broadband transmission system;

Figure 2 the internal structure of an ATM cell that is transmitted from a sender to a receiver via the serial data flow shown in Figure 1;

Figure 3a an illustration of the basic data flow according to the ATM transmission principle; and

Figure 3b is a schematic illustration of a known ATM broadband transmission system.

DESCRIPTION OF THE PREFERRED EMBODIMENTS

Figure 1 schematically shows the structure of a preferred exemplary embodiment of the inventive ATM transmission system. Viewed from the outside, this structure essentially corresponds to the known structure shown in Figure 3B. A sender/transmitter ~~transmission means~~ S receives a plurality of data channels K_0-K_3 as well as a clock signal T and converts the digital data of these data channels pending at it in parallel into a serial data stream D that is composed of a plurality of successively transmitted ATM cells. This serial data stream D is received by a receiver ~~reception means~~ E and

interpreted and allocated at the output side to the data channels K_0-K_3 of the output side. A special characteristic of the exemplary embodiment shown in Figure 1, however, is the fact that the sender ~~transmission means~~ S is supplied with four data channels K_0-K_3 whose digital data are acquired parallel in four-bit fashion and converted into the serial data stream, i.e. multiplexed. The sender S ~~transmission S means~~ optically transmits the serial data stream to the receiver ~~reception means~~ E via a light waveguide arrangement. The individual data channels K_0-K_3 can, for example, exhibit a transmission rate of 830 Mbit/s, whereas the serial ATM data stream is optically transmitted ~~with a~~ corresponding data ~~rate~~ of 3.3 Gbit/s ~~in accord therewith~~.

The parallel read-in of the digital data of the four data channels K_0-K_3 in four-bit fashion is particularly advantageous -- as shall be explained in greater detail later -- because the four bits of the individual data channels K_0-K_3 read-in in parallel can be combined especially easily in the sender ~~transmission means~~ S to form data units in the form of half-bytes that are transmitted from the sender ~~transmission means~~ S to the receiver ~~reception means~~ E in the form of ATM cells. According to the exemplary embodiment shown in Figure 1, each ATM cell of the series in a ~~[sic]~~ data stream D to be transmitted accordingly comprises a plurality of serially transmitted half-bytes that each respectively comprise a bit read-in in parallel from each data channel K_0-K_3.

The structure of the ATM cells of the serial data stream D transmitted from the sender ~~transmission means~~ S to the receiver E is ~~reception means E shall be~~ explained in greater detail below with reference to Figure 2. This is thereby a matter of a preferred example of a cell format employed by the assignee for a multicast mode. Of course, other ATM cell formats are also possible.

The ATM cell shown in Figure 2 comprise~~s~~ the standardized ATM cell structure as initially already set forth with 53 octets ~~or, respectively,~~ bytes, which are ~~these being~~ formed by the octets Nos. 10-62 in Figure 2. This standardized cell structure is referenced "external ATM cell" in Figure 2 and comprises, first, an "external" header as well as the previously ~~aforementioned~~ information field in which ~~wherein~~ the actual payload information is contained. The "external" header comprises 5 octets, and ~~whereas~~ the information field comprises 48 octets.

According to Figure 2, the ~~transmission means~~ sender S shown in Figure 1 attaches additional address ~~or, respectively,~~ / control octets that comprise internal routing information for the transmission of the ATM cells between the individual switching modules to this standardized ATM cell structure having 5 header octets and 48 information field octets. According to Figure 2, these internal address or, respectively, control information comprises an "internal" header with an additional 10 octets as well as an "internal" trailer with one octet that terminates the ATM cell, so that the ATM cells to be transmitted overall from the transmitter S to the receiver E comprise a total of 64 octets ~~or, respectively,~~ / bytes. As has already been explained on the basis of Figure 3, it is ~~already~~ fundamentally known to attach additional address or control octets with routing information for the transmission to the 53 octets prescribed according to the standard.

Inventively, however, it is now proposed that a characteristic bit sequence that can be unambiguously identified within each ATM cell at the reception side be transmitted within the ATM cell. The receiver monitors the serial data stream provided to it for the occurrence of this characteristic bit sequence and, after recognizing this characteristic bit sequence, can identify and determine the start of the corresponding ATM cell within the serially transmitted data stream. This is particularly possible according to the present invention because the bits of the digital data channels K_0-K_3 read-in in parallel at the transmission side (see Figure 1) are combined into data units, each of which ~~whereby each data unit~~ comprises an identical plurality of bits from each data channel. The bits of each data channel always have the same position within the individual data units, so that -- after identifying the characteristic bit sequence in the receiver -- the beginning of the first data unit of the corresponding ATM cell, i.e., the position of the individual data units in the serial optical data stream, can be determined, and the individual bits of the individual data units can be correctly divided onto the individual data channels K_0-K_3 at the output side.

It would be fundamentally possible that the individual, serially transmitted data units of each ATM cell comprise two or more bits from each data channel K_0-K_3, in which ~~whereby~~, for example, the bits 0 and 1 are allocated to the data channel K_0, the bits 2

and 3 are allocated to the data channel K_1, etc. In this case, the data units to be transmitted would be respectively formed by a full byte, by which ~~whereby~~ each ATM cell would be correspondingly transmitted byte-by-byte from the transmitter to the receiver.

However, it is advantageous to respectively read only one bit in in parallel from each data channel K_0-K_3 at the transmission side dependent on the supplied clock signal T (see Figure 1) and to multiplex them, so that the data units of the serial data stream transmitted from the transmitter /sender S shown in Figure 1 to the receiver E are respectively formed by half-bytes with four bits, where ~~whereby~~ 128 serially transmitted half-bytes form an ATM cell of the serial data stream D according to Figure 2. In other words, this means that each octet of the ATM cell shown in Figure 2 is preferably transmitted from the transmitter /sender S to the receiver E in half-bytes by transmission of a half-byte HB0 and of a following, second half-byte HB1. The arrow shown in Figure 2 ~~thereby~~ corresponds to the transmission sequence of the individual half-bytes HB0 and HB1.

In order for ~~So that~~ the bits contained in the individual half-bytes to ~~can~~ be correctly acquired at the receiver side and divided onto the data channels K_0-K_3 of the output side, the receiver E must determine, first, the respective beginning of the individual ATM cells and, second, the beginning of every half-byte within each ATM cell in the data stream D having successively transmitted half-bytes that is supplied to it.

INS a9 ~~As has already been explained, a characteristic bit sequence that is~~ monitored for occurrence at the receiver side is transmitted within each ATM cell for this purpose. This characteristic bit sequence is always transmitted at the same location in each of the transmitted ATM cells, i.e., in the same octet and divided onto the same half-bytes. When, thus, the receiver recognizes the occurrence of this characteristic bit sequence in the serial data stream D supplied to it, the receiver can ~~it can~~ -- since it knows the relationship between the position of the characteristic bit sequence within the ATM cell and the beginning of the ATM cell, i.e., the position of the ATM cell within the serial data stream -- determine the beginning of the corresponding ATM cells and, thus, the first half-byte of this ATM cell in the serial data stream and can correctly divide the individual bits of this first half-byte as well as of the following half-

bytes of the corresponding ATM cell successively onto the individual data channels K_0-K_3 of the output side, so that these are output correspondingly parallel.

Due to the fact that a bit sequence that is already contained and transmitted in the ATM cell format shown in Figure 2 is employed as characteristic bit sequence of each ATM cell, no additional data outlay arises for the receive-side synchronization, i.e., allocation of the individual bits of the serial data stream to the corresponding data channels K_0-K_3 of the output side, i.e., no additional synchronization information need be attached to the actual serial data stream D to be transmitted, so that no redundancy occurs.

Advantageously, the first octet of each and every ATM cell can be employed as the above-described, characteristic bit sequence. Given employment of the cell format shown in Figure 2, this octet 0 shown in Figure 2 is required in standardized fashion in the ATM broadband transmission systems shown in Figures 1 and 3 for the interpretation and determination of the corresponding ATM cell in the individual switching modules (transmitter, receiver) and is referred to a synchronous octet. This synchronous octet comprises bits consecutively numbered with 0 through 6 in Figure 2 that have the same value for each ATM cell to be transmitted and are thus fixed. The ~~more~~ most significant bit 7 of this synchronous octet, which is referenced T in Figure 2, is a toggle bit that the transmitter sets in alternation from ATM cell to ATM cell. Advantageously, this synchronous octet already transmitted with the ATM cell format shown in Figure 2 is employed as characteristic bit sequence whose occurrence in the serial data stream is monitored by the receiver. As soon as the receiver E shown in Figure 1 has recognized the occurrence of this bit sequence of the synchronous octet in the serial data stream D, it ~~surmises~~ presumes that this is the beginning of a new ATM cell that comprises 64 octets overall, including the synchronous octet, so that the receiver E can interpret the individual octets of the corresponding ATM cell transmitted by half-bytes. As shown in Figure 2, of course, the synchronous octet is also transmitted by half-bytes according to the preferred exemplary embodiment, i.e., the four less significant bits 0-3 of the synchronous octet are serially transmitted within

a first half-byte HB0 and the four more significant bits 4-7 are serially transmitted in a following half-byte HB1.

The relationship of the bits combined in the half-bytes HB0 or, respectively, HB1 and the corresponding data channels is also shown in Figure 2. The ~~As has already been explained, the~~ individual octets 0-63 of every ATM cell are transmitted from the transmitter to the receiver by half-bytes on the basis of the successive transmission of a first half-byte HB0 and of a second half-byte HB1. Each of these half-bytes HB0, HB1 comprises four bits read in in parallel from the data channels K_0-K_3 adjacent at the transmitter S (see Figure 1). A bit position is ~~thereby~~ allocated to a fixed data channel within each half-byte HB0, HB1. According to Figure 2, for example, the bit 0 of each half-byte HB0 or HB1 thus always corresponds to the data channel K_0, whereas, for example, the bit 2 corresponds to the data channel K_2. The receiver E can thus simply demultiplex the serial bit sequence supplied to it, since, after recognizing the occurrence of the synchronous octet in the serial data stream, it knows the beginning of the first half-byte of the corresponding ATM cell, so that -- according to the allocation shown in Figure 2 -- it must simply successively distribute respectively one bit onto the data channels K_0-K_3 of the output side so that the parallel data channels adjacent at the input side again appear correctly at the output of the receiver.

The function of the individual component parts of the ATM cell format shown in Figure 2 shall be briefly explained below by way of addition.

As has already been explained, the "internal" header attached to the standardized ("external") ATM cell format having a total of 53 octets comprises a total of 10 octets 0-9. The individual octets of this "internal' header comprise routing information for the transmission of the corresponding ATM cells. Some bits R that are currently not yet used, and are thus reserved, are present within this internal header. The bits referenced SSN (switching state number) serve the purpose of designationally transmitting the corresponding ATM cell to a specific switching element. For example, a specific switching element can thus recognize on the basis of the information of this SSN bit field whether the respective ATM cell is intended for the

corresponding switching element. The bits referenced CF define the currently still unused flag (congestion flag). Further more, the internal header contains a parity bit P for a parity check of the routing information contained in the internal header. AUX references auxiliary bits. The bits MCRA reference the internal routing address of the corresponding ATM cell (multicast routing address). The bits HK (housekeeping) serve for the classification of the cell (dummy cell, etc.). The bits ADI (address identifier) serve for defining addresses for a physical multicast mode in the individual switching elements. Delay priorities can be defined for the individual ATM cells with the assistance of the bits CDP (cell delay priority). The octets of the internal header referenced SN (sequence number) serve for consecutive numbering of the individual, serially transmitted ATM cells. The bits referenced RMS (redundant module sender) and RMR (redundant module receiver) are special bits for a farther-reaching redundancy classification of the individual ATM cells. This is especially meaningful because all ATM cells are fundamentally transmitted twice for security reasons.

The internal trailer that is likewise attached to the standardized cell format (octet 10-62) at the end comprises a checkbit sequence referenced FCS2 (frame check sequence) for the payload information transmitted in the information field.

The structure of the "external" header with the standardized 5 octets 10-14 is notoriously known, ~~so that this shall~~ and will not be discussed further here. In general, this external header contains address information MCI (multicast connection identifier) and VCI (virtual channel identifier). Further more, the type of payload transmitted in the information field is referenced PTI (payload type identification) and the corresponding ATM cell has a specific cell priority (CLP, cell loss priority) allocated to it. Finally, the external header contains a further check octet (FCS1, frame check sequence) that serves for checking both the external header (octet 10-14) as well as the octets 2-9 of the internal header.

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~~List of Reference Characters~~

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~~S~~	~~transmission means~~
~~E~~	~~reception means~~
D	serial data stream
~~K_0-K_3~~	~~parallel data channels~~
~~T~~	~~clock signal~~
~~Z~~	~~ATM cell~~